ATAL FDP - RECENT TRENDS IN SEMICONDUCTOR SYSTEM DESIGN AND TESTING TECHNIQUES

Event No	EC001
Organizing Department	Electronics and Communication Engineering
Date	05/02/2024 to 10/02/2024 (6 Days)
Time	09:00 AM to 05:00 PM
Event Type	FDP
Event Level	Dept. Level
Venue	Veena Hall
Total Participants	39
Faculty - Internal	11
Faculty - External	19
Students - Internal	6
Other Participants	3

Related SDG

Resource Persons

Sl	Type	Name	Designation	Company	Email	Phone
1	Resource Person	Dr A Senthilkumar	Dean (Academic and Autonomous) & Senior Professor	Dr. Mahalingam College of Engineering & Technology	deanaa@drmcet.ac.in	xxxxxxxxxx
2	Resource Person	Dr Sakthivel R	Associate Professor Grade 2	Vellore Institute of Technology	rsakthivel@vit.ac.in	xxxxxxxxxx
3	Resource Person	Dr M Senthil Sivakumar	Assistant Professor	Indian Institute of Information Technology	msenthilsivakumar@iiitt.ac.in	xxxxxxxxxx
4	Resource Person	Dr D Suresh	Assistant Professor	Indian Institute of Information Technology	sureshd@iiitt.ac.in	xxxxxxxxxx
5	Resource Person	Dr Suresh Balanethiram	Assistant Professor	National Institute of Technology	suresh.b@nitpy.ac.in	xxxxxxxxxx
6	Resource Person	Dr Mamidi Nagaraju	Technical Manager	Entuple Technologies	nagaraju.m@entuple.com	xxxxxxxxxx
7	Resource Person	Dr Bhaskar M	Professor	National Institute of Technology	bhaskar@nitt.edu	xxxxxxxxxx
8	Resource Person	Mr B K Shivaprasad	Sr. Field Application Engineer	Entuple Technologies	shivaprasad.bk@entuple.com	xxxxxxxxxx
9	Resource Person	Mr V Navaneethakrishnan	Sr. Field Application Engineer	Entuple Technologies	navaneethakrishnan.v@entuple.com	xxxxxxxxxx

Involved Staffs

Sl	Name	Role
1	Indra J	Coordinator
2	Muralidharan J	Coordinator

Outcome

The outcome of Recent trends in semiconductor system design and testing is Continued advancements in process technologies, such as EUV lithography and novel materials, which have enabled the production of semiconductor devices with smaller feature sizes, higher integration densities, and improved performance. There has been a focus on integrating diverse semiconductor components (e.g., CPUs, GPUs, accelerators) on a single chip or package to enhance performance, reduce power consumption, and improve system-level efficiency. Automation tools and methodologies have evolved to streamline the design process, reduce design time, and enhance productivity. This includes the development of advanced design automation software, verification techniques, and modeling frameworks. Efforts to improve semiconductor reliability have led to the development of new reliability modeling techniques, fault simulation methods, and testing methodologies. This has helped to identify and mitigate potential failure mechanisms, enhancing product quality and longevity. With growing concerns about cybersecurity, semiconductor designs now incorporate more robust security features, including hardware-based security mechanisms, cryptographic accelerators, and tamper-resistant designs, to protect against threats such as side-channel attacks and counterfeiting. Testing methodologies have evolved to address the challenges posed by complex semiconductor designs, including developing new test architectures, built-in self-test (BIST) techniques, and fault diagnosis algorithms. These innovations have helped improve test coverage, reduce test time, and enhance manufacturing yield.

Event Summary

The ATAL FDP on 'RECENT TRENDS IN SEMICONDUCTOR SYSTEM DESIGN AND TESTING TECHNIQUES' is scheduled from 05.02.2024 to 10.02.2024. The FDP was inaugurated by our beloved Principal Dr. D. Saravanan in the presence of Dr. M. Kathirvelu, HoD, ECE along with faculty members and participants. The first session was handled by Dr.A.Senthilkumar, Dean (Academic and Autonomous),Senior Professor, Department of EEE,Dr. Mahalingam College of Engineering & Technology, Pollachi on the topic Reconfigurable Hardware architectures. Then the afternoon session was handled by Dr. Sakthivel R, Associate Professor Grade 2, Department of Micro and Nanoelectronics, School of Electronics Engineering, Vellore Institute of Technology Vellore on the topic VLSI Architecture. The Day 2 was handled by Dr. M. Senthil Sivakumar & Dr. D. Suresh, Assistant Professor, Department of ECE, Indian Institute of Information Technology, Tiruchirappalli on the topic VLSI System Design Testing and Validation & VLSI Phase change Memory Devices respectively. Day 3 was handled by Dr. Suresh Balanethiram Assistant Professor, Department of ECE, National Institute of Technology, Puducherry on the topic Compact modeling and continued by Dr. Mamidi Nagaraju, Technical Manager, (ASIC Design and EDA Support), Entuple Technologies, Bengaluru on the topic UART Design and Prospect. During the Day 4 the topic Low Power VLSI Circuit Design was handled by Dr. Bhaskar M, Professor, Department of ECE, National Institute of Technology, Trichy and ASIC Design Flow by Mr. B. K. Shivaprasad, Sr. Field Application Engineer, Entuple Technologies, Bengaluru. The industrial visit to VVDN technologies, Arutchelvar Advanced Technology Center, 6th Floor, Diamond Jubilee Building Dr. MCET Campus, Udumalai Road, Pollachi, Coimbatore, TamilNadu – 642003 was planned for participants on day 5 as a part of FDP. The afternoon session is on LEON Processor Architecture and Design by Mr. V. Navaneethakrishnan, Sr. Field Application Engineer, Entuple Technologies, Bengaluru. The last day of FDP event started with a session on Stress Management by Mr. S. Satheesh Kumar, Assistant Professor (Sr.G.), Department of ECE, KPR Institute of Engineering and Technology, Coimbatore. Then the FDP event continued with Reflection Journal session, Assessment (MCQ), Feedback collection Interactions with the participants and concluded with a Valedictory function. The article discussion session was carried out on Day 1 to Day 4. The hands-on training session was provided to participants from Day 1 to Day 5.

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